REMARKS/ARGUMENTS

Claims 1-3, 5-7 and 9-14 are pending. Claims 1, 9 and 14 have been amended, and claims 4 and 8 have been cancelled. Reconsideration is respectfully requested.

1. Rejection of Claims 4, 8, 13-14, 9 and 12 Under §112

Claims 4, 8, 13-14, 9 and 12 were rejected under 35 U.S.C. 112, first paragraph. The Advisory Action of February 18, 2010 indicates this rejection has been overcome.

2. Rejection of Claims 9 and 12 Under §102(b)

Claims 9 and 12 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication 2001/0033278 (Ohta). The Applicant respectfully traverses this rejection.

Claim 9, as amended, recites a drive circuit for controlling n rows of a display device that is operable in a partial mode, where the row drive circuit includes, among other things, a logic function connected in front of each of n outputs of a shift register. The logic function is configured to deactivate the n outputs of the shift register in dependence on the partial mode responsive to and during one or more pulses of a first control signal by preventing the n outputs of the shift register from driving the n rows of the display device. The outputs of the shift register are activated consecutively in dependence on pulses of a clock signal, ***where the frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.*** Claim 12 similarly recites sequentially providing an enable signal to enable each row in response to clock signal pulses, and deactivating row outputs during a first control signal first pulse, ***where the frequency of the clock signal pulses increases during the first control signal pulse***. The relationship between the increased frequency of the clock pulses during the (one or more) first control signal pulse(s) is illustrated in Fig. 3, and described on page 4, lines 7-31.

Ohta discloses a display device driving circuit that includes an output pulse control section 37b that deactivates the operation of the bi-direction shift register sections 33 through 36

in response to the GCNT2 signal (paragraph [0051]). However, there is no teaching or suggestion of operating the shift register sections using a clock signal that increases in frequency during the (one or more) control signal pulses. In fact, Ohta specifically teaches away from such a configuration by decreasing the frequency of the clock signal for the non-display portions of the liquid crystal panel (see paragraphs [0065] and [0076]). Therefore, it is respectfully submitted that claims 9 and 12, as amended, are not anticipated by Ohta, and that this rejection should be withdrawn.

3. Rejection of Claims 1-8, 10-11 and 13-14 Under §103(a)

Claims 1-8, 10-11 and 13-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta. Claims 4 and 8 have been cancelled. The Applicant respectfully traverses this rejection with respect to the remaining claims.

Claim 1 has been amended to include the features of claims 4 and 8 (which have been cancelled). Claim 1, as amended, recites, among other things, a logic function in the row drive circuit in front of the row outputs configured to prevent the n outputs of the shift register from driving any of the n rows of the display responsive to and during the one or more pulses of the first control signal, where the clock signal (on which the consecutive activation of the shift register outputs depend) ***increases in frequency during the one or more pulses of the first control signal.*** As stated in Part 2 above, not only does Ohta fail to teach or suggest increasing the clock signal during the pulse(s) of the first control signal, but in fact Ohta teaches away from this claimed feature by decreasing the frequency of its clock signal for the non-display portions of the liquid crystal panel (see paragraphs [0065] and [0076]).

On page 9 of the Office Action, the Examiner states (with respect to claim 8) that Ohta teaches the frequency of the clock signal (GCK) "can be increased in a case of one or several consecutive rows (i.e. non display portion 1a, 1b) that is or are not to be displayed ([0065])." The Applicant respectfully traverses this conclusion, because paragraph [0065] of Ohta set forth below specifically teaches the opposite:

> **[0065]** Here, the display data signals for the non-display portions **1***b* and **1***c* are used to charge the respective pixels by applying a voltage to the plurality of pixels with respect to a single data signal line. This might result in deficiency in amount of charge if the duration of voltage application is not different from normally, which, nonetheless, poses no serious problem since it occurs equally in all pixels and thus less color non-uniformity is caused on the non-display portions **1***b* and **1***c*. Nevertheless, in order to secure a sufficient quantity of charge for the pixels in the non-display portions **1***b* and **1***c*, the display data signals may be applied to the respective pixels longer than usual, for example, by increasing the cycle time of the source clock SCK for the control **IC 4**, i.e., by decreasing the frequency, so as to increase the pulse width of the gate clock signal GCK.

Paragraph [0065] of Ohta clearly teaches decreasing the frequency of the clock for the non-display portions 1b and 1c, not increasing as stated by the Examiner.

Therefore, it is submitted that claim 1 (as amended), and claims 2-3, 5-7, 10-11 and 13-14 dependent thereon, are not rendered unpatentable over Ohta, and that this rejection should be withdrawn.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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